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DESIGN AND IMPLEMENTATION OF LOW POWER BCD ADDER ON FPGA

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ABSTRACT

A low-power 32-bit Binary-Coded Decimal (BCD) adder based on the Carry Lookahead Adder (CLA) architecture. It is designed for high-speed and power-efficient operation. The design targets applications that need precise decimal computation, such as financial and embedded systems. To reduce power consumption, it uses Power Gating, which lowers leakage current by turning off inactive circuit blocks. Power Gating performs better than Clock Gating when it comes to reducing leakage power, especially in wider data-path designs. The architecture is modeled in Verilog HDL, simulated with Xilinx Vivado and implemented on an FPGA platform for functional testing. Results show considerable improvements in power efficiency and operational speed, confirming that the CLA-Power Gating approach is suitable for low-power VLSI arithmetic units.

KEYWORDS

Binary-Coded Decimal (BCD) adder, Carry Lookahead Adder (CLA), Power gating, Low power VLSI, FPGA implementation, Verilog HDL, Leakage power reduction and Xilinx Vivado.

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INTRODUCTION

In modern digital systems, especially in financial and embedded applications, efficient decimal computation is essential. Binary-Coded Decimal (BCD) adders are crucial in these systems because they enable precise arithmetic operations without errors from binary-to-decimal conversion. However, traditional adder designs, like Ripple Carry Adders (RCAs), face delays due to carry propagation.

To increase speed, this project uses a Carry Lookahead Adder (CLA) design, which shortens carry propagation time and improves performance. For low power use, Power Gating is applied to cut down leakage power by disconnecting inactive logic blocks from the supply. In contrast to Clock Gating, which only reduces dynamic power, Power Gating better controls leakage, making it ideal for large data-path designs like the 32-bit BCD adder.

The design is outlined in Verilog HDL, simulated using Xilinx Vivado and tested through FPGA implementation. In this paper, the proposed Power Gating technique CLA-based 32-bit BCD adder shows significant gains in speed and power efficiency, aiding low-power VLSI design.

LITERATURE REVIEW

Several studies have looked at improving the speed and power use of arithmetic circuits, particularly adders. Traditional Ripple Carry Adders (RCA) are simple, but they have high delays because of how carries are passed through the circuit. CLA-based adders were created to solve this problem; they achieve faster addition by generating carries simultaneously.

Power-saving techniques like Clock Gating and Power Gating are well-known in low-power VLSI research. Clock Gating reduces dynamic power effectively, but it does not address leakage. On the other hand, Power Gating can lower static power significantly, even though it adds complexity in terms of area and wake-up delays.

Previous work has built BCD adders using hybrid designs and correction logic. However, many of these designs do not integrate high-speed architecture with strong leakage control effectively, especially for wider designs like 32-bit BCD adders. This project addresses that issue by combining CLA and Power Gating, implemented and validated through FPGA simulation.

Evolution of Adder Architectures

Digital adders are key parts of arithmetic logic units (ALUs). The Ripple Carry Adder (RCA) has a simple design, but it has a high propagation delay because carry generation happens one after the other. To solve this problem, the Carry Look Ahead Adder (CLA) was developed. The CLA greatly cuts down on carry propagation delay by generating carry signals ahead of time using generate (G) and propagate (P) functions, which makes it suitable for fast applications. Other types, such as Carry Skip Adders (CSA) and Carry Select Adders (CSLA), have been suggested to balance speed, area, and power use[1].

Review of Low Power Design Techniques

Power consumption in CMOS circuits is a major concern, especially for portable and embedded systems. Clock Gating reduces dynamic power by turning off the clock signal to inactive modules, but it does not significantly lower static leakage power[2].

Power Gating uses sleep transistors to completely cut off power to idle blocks, which effectively reduces leakage current. Newer power gating techniques, like dual recycled charge gating, have shown significant leakage reduction in arithmetic units.

Existing BCD Adder Designs

Binary Coded Decimal (BCD) adders are used in applications that need decimal digit operations, like financial and commercial systems[3]. Traditional BCD adders perform binary addition first. If the sum exceeds 9, a correction step follows. Researchers have suggested using optimized correction logic and fast binary adders like Carry Lookahead Adders (CLA) to improve performance. However, many existing designs mainly prioritize speed or accuracy. They offer little focus on making power-efficient solutions, especially for higher bit-widths, such as 32-bit[4].

Previous Work

Most of the existing research has focused on improving speed in BCD adders by using fast designs like CLA, CSLA and CSA. At the same time, low-power methods like Clock Gating and Power Gating have been studied on their own. However, very few studies have combined high-speed designs with power-saving techniques in BCD arithmetic circuits. Additionally, there is limited research on designing and implementing 32-bit BCD adders that use CLA and Power Gating techniques, especially with the goal of achieving both low power and high performance. This drives the proposed work, which aims to design a 32-bit BCD Adder using CLA along with Power Gating to lower power and increase speed.

PROPOSED METHODOLOGY

The overall 32-bit adder is divided into eight identical blocks. Each block handles 4 bits of the BCD input. These blocks contain a 4-bit binary adder that uses CLA, BCD correction logic to fix invalid BCD sums, and carry-out logic to send the carry to the next block. This modular design makes implementation easier and allows for reuse in larger projects.

Schematic diagram of 32-Bit BCD Adder

The schematic of the 32-bit BCD adder includes eight connected 4-bit BCD adder blocks. Each block carries out binary addition and has BCD correction logic. Each block uses Carry Lookahead Adder (CLA) architecture, which helps reduce propagation delay and improve performance. To lower leakage power, power gating is added with sleep transistors that are controlled by a gating signal. This setting allows for idle blocks to be turned off selectively. This design is efficient arithmetic operations.

BCD Adder Block function

Each 4-bit BCD adder takes two 4-bit inputs and a carry-in to perform binary addition. If the result exceeds 9 or generates a carry, a correction value of 6 (0110) is added to ensure the output stays within the valid BCD range. The corrected result is then used as the sum, while any carry goes to the next BCD digit block, keeping accuracy across the full 32-bit width.

CLA Integration

To improve performance, the binary adder in each BCD block uses Carry Lookahead Adder (CLA) logic. This technique speeds up addition by calculating carry signals at the same time, instead of one after another like Ripple Carry Adders. Using CLA greatly reduces propagation delay, making the adder faster and better for high-speed arithmetic operations.

Power Gating in Schematic

Each 4-bit BCD adder unit includes a sleep transistor (PMOS or NMOS), which is managed by a Power Gating Control Unit. When a specific block is inactive, the control signal turns off the sleep transistor. This effectively cuts the power supply and reduces leakage currents. This method improves energy efficiency without impacting performance during active computation.

The design takes two 32-bit BCD operands and an initial carry-in signal. It also has a power gating control input to turn blocks on or off.

The outputs include a 32-bit BCD sum and a final carry-out, along with optional status indicators such as overflow or enable signals to improve system integration.

RESULTS AND DISCUSSION

This section presents the simulation results, timing performance and power consumption of the proposed 32-bit BCD Adder, which is implemented using CLA and power gating techniques. The design is developed in Verilog HDL and simulated using Xilinx Vivado to ensure functional correctness and assess power usage.

Simulation Waveform

The Verilog design was simulated with different BCD inputs using a custom testbench to check its functionality.

The waveform results show proper carry propagation in the 4-bit BCD blocks and correct BCD correction logic after each addition stage. Both edge cases, such as sums greater than 9, and regular decimal additions were tested. The output waveforms confirmed accurate 32-bit BCD results and carry propagation.

The waveform shows the functional simulation of the 32-bit BCD Adder using Carry Lookahead logic and Power Gating. It displays the input operands, intermediate carries, correction logic, and the final BCD output.

Power Analysis(with and without Power Gating)

Power analysis examined both static and dynamic power use. The results indicated that enabling power gating significantly lowered static (leakage) power, particularly when specific blocks were idle.

In contrast, without power gating, leakage increased notably, especially with larger input ranges. Dynamic power, however, stayed fairly consistent in both situations. The suggested method is very effective at cutting standby power, which is important for battery-operated or energy-limited systems.

The table compares the static and dynamic power consumption of the 32-bit BCD Adder in two scenarios. One scenario has no power-saving technique. The other scenario uses a Carry Look ahead Adder (CLA) with Power Gating.

Table No.1: Comparison of static and dynamic power

S.No	Technique	Static Power (W)	Dynamic Power (W)
1	32-bit BCD Adder Without Gating	0.227	25.387
2	32-bit BCD Adder With CLA Power Gating Technique	0.225	25.160

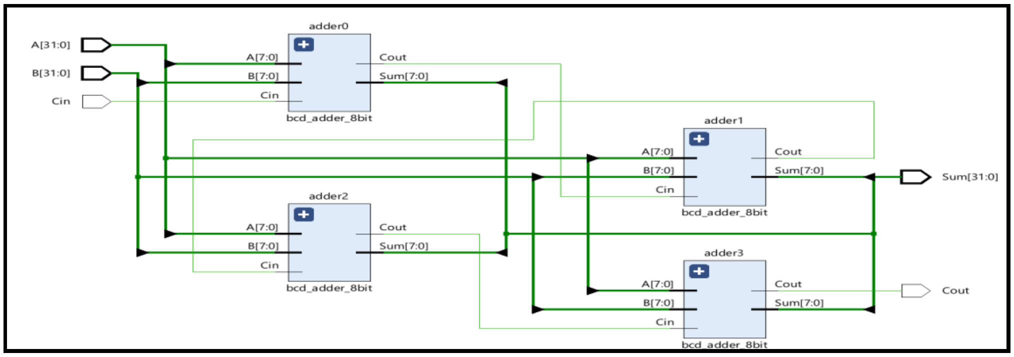


Figure No.1: RTL Schematic diagram of 32-bit BCD Adder

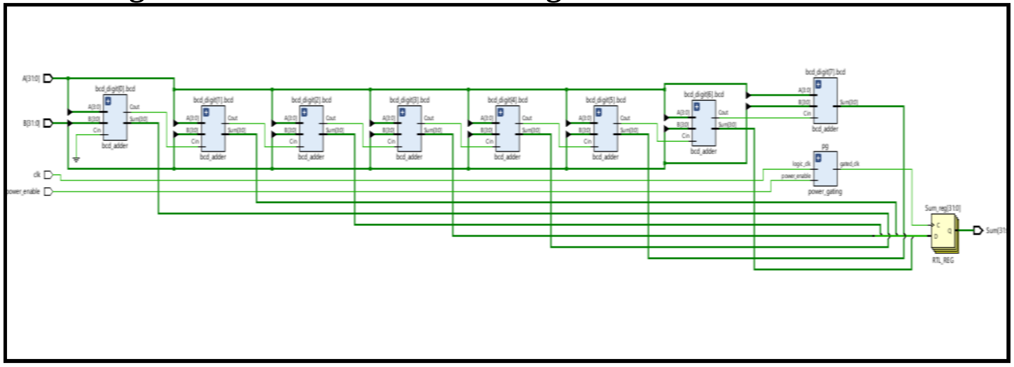


Figure No.2: RTL Schematic diagram of 32-bit BCD Adder using CLA Power Gating Technique

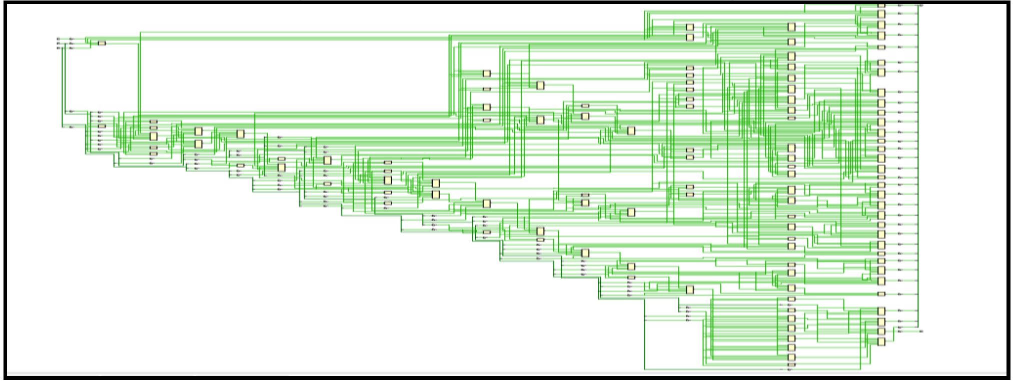


Figure No.3: RTL Netlist of the 32-bit BCD Adder without Gating

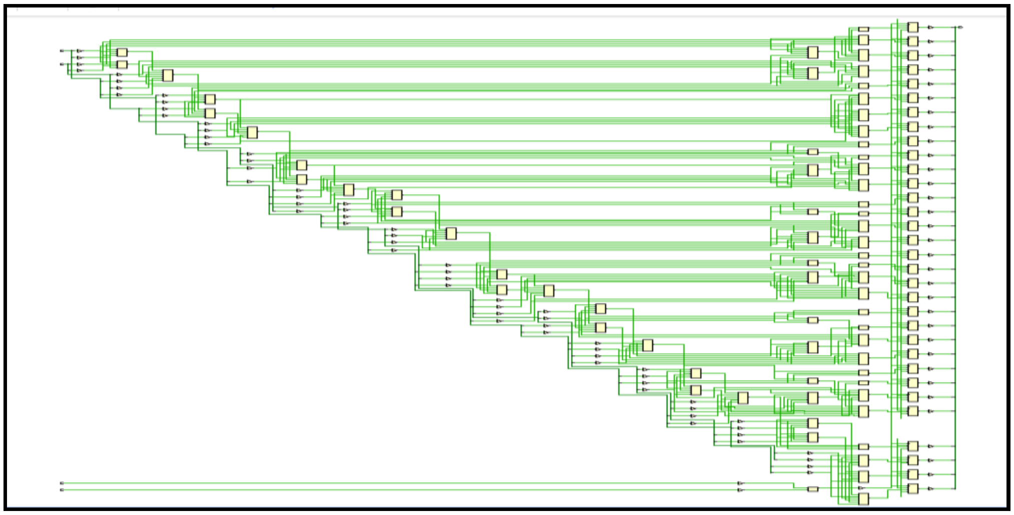


Figure No.4: RTL Netlist of the 32-bit BCD Adder using CLA and Power Gating Technique

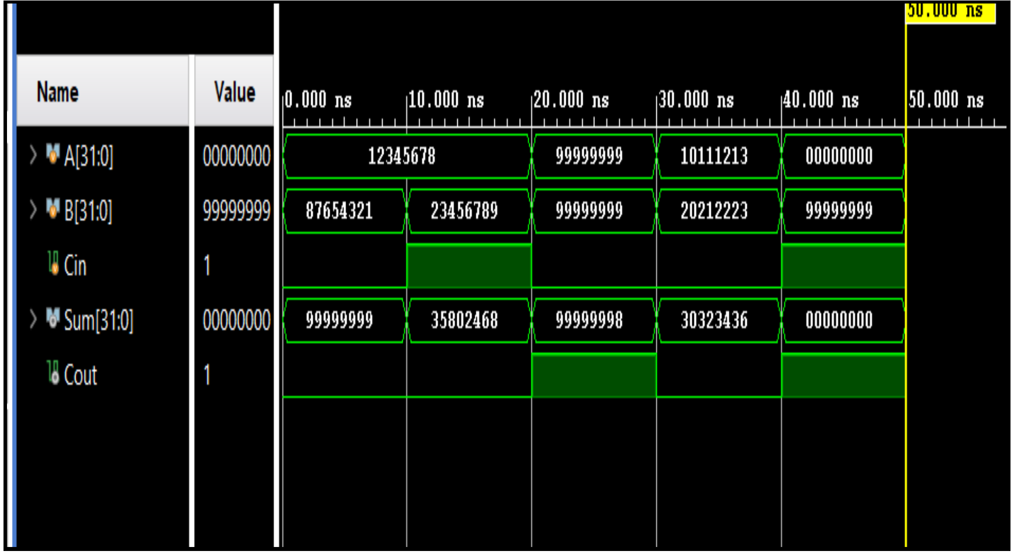


Figure No.5: Waveform Output of 32-bit BCD adder without gating

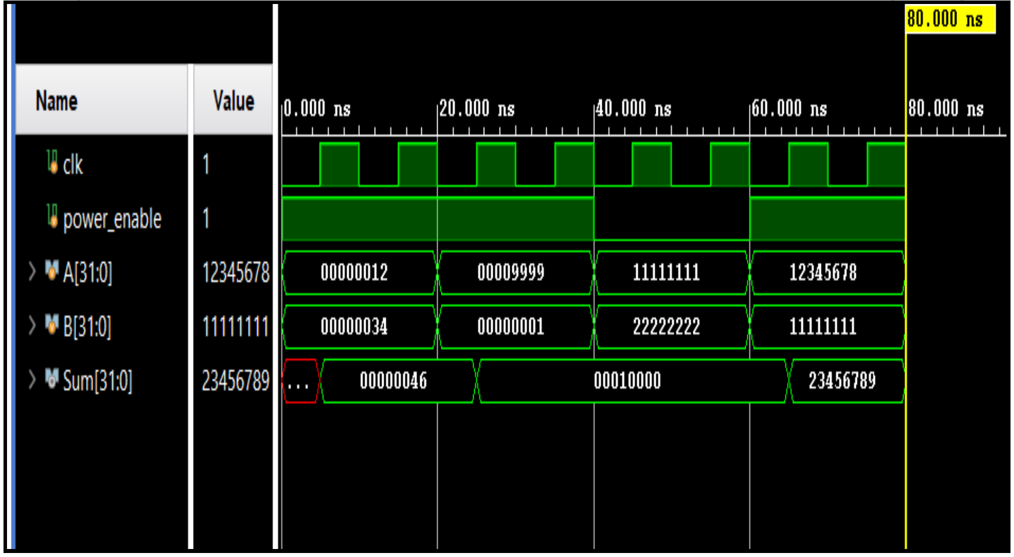
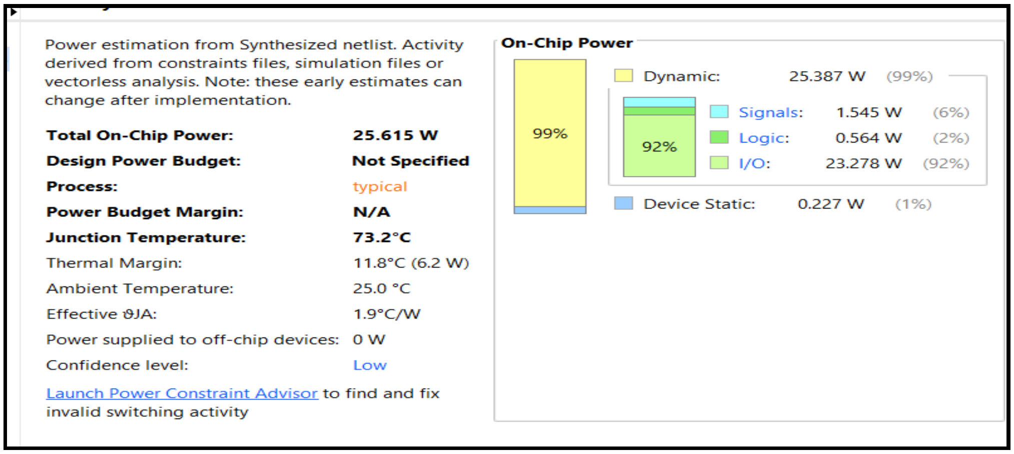


Figure No.6: Waveform Output of 32-bit BCD Adder using CLA Power Gating Technique



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

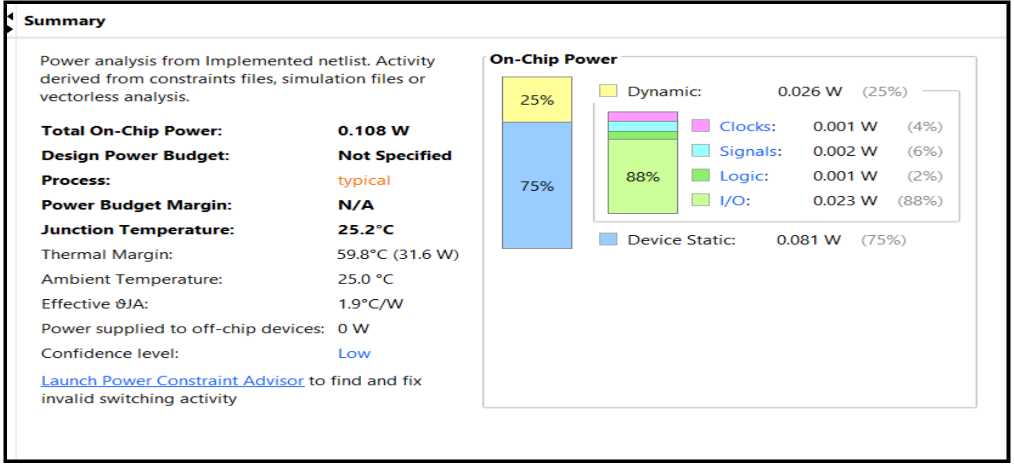
Total On-Chip Power:	**25.615 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**73.2°C**
Thermal Margin:	11.8°C (6.2 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	25.387 W	(99%)	
	Signals:	1.545 W	(6%)
	Logic:	0.564 W	(2%)
	I/O:	23.278 W	(92%)
Device Static:	0.227 W	(1%)	

Figure No.7: Power Consumption of 32-bit BCD Adder without gating



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.108 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.026 W	(25%)	
	Clocks:	0.001 W	(4%)
	Signals:	0.002 W	(6%)
	Logic:	0.001 W	(2%)
	I/O:	0.023 W	(88%)
Device Static:	0.081 W	(75%)	

Figure No.8: Power Consumption of 32-bit BCD Adder using CLA power gating technique

CONCLUSION

This work presents a 32-bit BCD adder using CLA architecture and Power Gating. It achieves high speed and low power. The design significantly lowers leakage power compared to Clock Gating while keeping the area and speed at acceptable levels. Simulation results confirm the advantages of the proposed architecture for energy-efficient arithmetic operations in embedded and financial applications. Future work may extend this design to ASIC implementations and explore adaptive power gating based on real-time workload.

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CONFLICT OF INTEREST

We declare that we have no conflict of interest.

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